**CSIR-CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE**
**PILANI – 333 031 (RAJASTHAN)**

No. COA/Committees/23(3) Date : 16/02/2024

**OFFICE MEMORANDUM**

**Sub: Reorganization of Labs.**

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In continuation of this office OM of even number dated 05/01/2024 and OM No.COA/Committees/22(26) dated 27/07/2022, the Director, CSIR-CEERI, Pilani has been pleased to reorganize the Labs. as under:-

1. IC Design Lab (IC Design Software) and IC Desing Testing Lab (Tecsting of ICs) has been reorganized as **"VLSI Design & FPGA Prototyping Lab".** This Lab will be operational in Room No. 51 and headed by Dr. Sanjay Singh, Head, Advanced Information Technologies Group.

2. Embedded System Design Lab (Embedded Software and FPGA/Evaluation Kits) and Embedded System Prototyping Lab has been reorganized as **"Embedded Systems Development Lab".** This Lab will be operational in Room No. 41 and headed by Dr. Udit Narayan Pal, Head, Societal Electronics Group.

3. Sensor & Microsystem Prototyping Lab has been reorganized as **"Sensor & Microsystems and Characterization Lab".** This Lab will be operational in Room No. 104 and headed by Sh. Ashok Chauhan, Head, Institute R&D Facilities Group.

   This OM will take immediate effect.

16/02/2024

**(Mahendra Singh)**
**Administrative Officer**

To:-

1. Dr. Sanjay Singh, Head, AIT Group
2. Dr. Unit Narayan Pal, Head, Societal Electronics Group
3. Sh. Ashok Chauhan, Head, Institute R&D Facilities Group

Copy to:-

1. All Section/Division Heads - Through website
2. Director's Secretariat - For information
3. AIT Group - Kindly upload this OM on the website of the Instt.
4. Notice Board