CSIR-CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE, PILANI

INTERVIEW SCHEDULE FOR THE POST OF PRINCIPAL SCIENTIST & SENIOR SCIENTIST

Interviews for the post of Principal Scientist (Post Code – CEERI-1) & Senior Scientist (Post Code – PMBD-1), advertised vide Advt. No. 03/2017, will be conducted as per the following schedule:

Post & Post Code	Date	Reporting Time
Principal Scientist (Post Code – CEERI-1)	26.10.2018	08:30 AM
Senior Scientist (Post Code – PMBD-1)	27.10.2018	08:30 AM

Venue of Interview:

CSIR-Recruitment & Assessment Board (CSIR-RAB)
CSIR Complex, Library Avenue, Pusa,
New Delhi – 110012.

Interview letters to the candidates recommended for interview are being sent to their correspondence addresses.

Interview schedule for the remaining Post Codes will be notified shortly.

INSTRUCTIONS

a) Candidates Called for Interview are allowed provisionally for appearing for interview subject to verification of all the required documents.

b) If a candidate is short-listed inadvertently and he/she is found ineligible at the time of the interview, neither he/she will be allowed for interview nor payment of TA will be made.

c) Candidates called for interview must bring with them the following documents at the time of interview:

1. Original Certificates and Mark Sheets (Yearwise/ Semesterwise, as the case may be) in support of educational qualifications alongwith one self-attested copy of each.
2. A 'No Objection Certificate' from the present employer, if applicable.
3. Documentary proof in respect of Date of Birth.
4. SC/ST/OBC/PwD certificate, if applicable, issued by appropriate authority in the format prescribed for employment in Central Government.
5. Certificate for OBC should be latest (issued after 31st March, 2018).
6. All relevant experience certificates, if applicable.

01/10/2018

SECTION OFFICER
Date: 01.10.2018