CSIR-CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE, PILANI

Brief Detail of Present Projects

S.No.	Area	Project Title/Work Package/Activity Name/Number	Brief description about the project
1.	CPS	GAP- 3413	Development of deep learning based recognition engine for low resolution images that results in robust and efficient recognition and retrieval from Indian language document images.
2	CPS	HCP0013- Vertical 2 (Heritage and Culture)	To develop 3D rendering system to construct the 3D view of given structure and also may be used for identify the defects in the structure. To simulate the structure by introducing defects and capturing their simulation results theoretically and validating them using sensor based simulation results.
3.	CPS	HCP0013 (Intestine Lung Disease)	This project is based upon the Texture based analysis can estimate lung function on morphological images and hence can be used for quantification. Texture based analysis can predict reversibility/ response to therapy. We develop algorithms for texture based analysis of lung from CT data to estimate lung function and diagnosis. We proposed the deep learning framework and the advance aspects such as use of GAN networks to overcome data limitations and provide analytical support.
4.	CPS	"Face Anti-Spoofing Solution"	Spoof attacks are an attempt to acquire someone else's privileges or access rights by using a photo, video or a different substitute for an authorized person's face. There are three popular ways of such attacks: Print/Display Photo Attack, Replay/Video Attack, and 3D Mask Attack. "Face Anti-Spoofing Solution" project aims at development for AI algorithms for detecting such spoofing attacks. Main objective of the project is to develop deep learning based algorithms for face liveness detection.
5.	CPS	GAP-3412 [Special Manpower Development Programme for Chip-to-Sytem Design (SMDP-C2SD)]	This is a multi-institutional (60 institutes across the country) programme and there are project implementation units (PIUs) located at CSIR-CEERI and MeitY for coordination and smooth functioning. The PIU@MeitY is responsible for maintenance and upkeep of EDA tools, system administration of worlstations, and technical coordination between MeitY, CSIR-CEERI, and other institutes (including IITs, IISc, NITs, etc.). It is also maintain the programme's website, update of activities/events, forums, workshops, meetings, etc. in addition to monitoring technical and financial progress at each of the 60 sites.